TMS
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Monsoon Mapping for Teststand

Goal: To map the Monsoon system (1 Controller Board, 1 Clock and Bias Board and 1 CCD Acquisition Board) which we will receive at FNAL into a teststand readout system capable of controlling the readout of up to 4 CCDs.

We will assume that all four CCDs can share clock rail settings for similar clock lines. Part of the testing exercise will be to determine if this is indeed true.

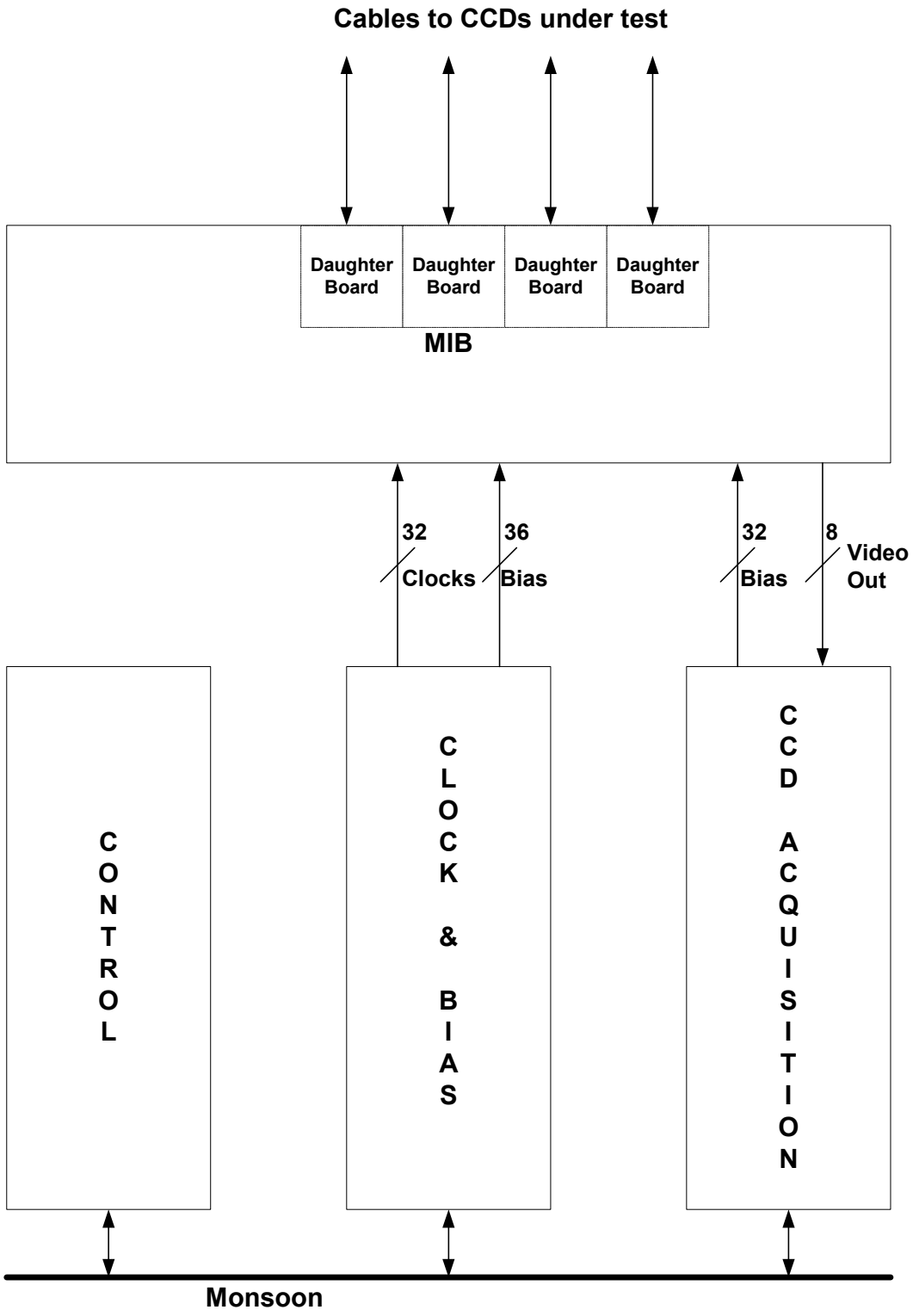
We will use the Monsoon boards and generic transition boards. A custom Monsoon Interface Board (MIB) will be designed. The MIB will receive 32 clock lines and 36 bias lines from the Clock and Bias board. It will also receive the 32 bias outputs of the CCD Acquisition Board. Video outputs will be driven from the MIB to the CCD Acquisition Board.

The MIB will contain CMOS switches and buffers used to drive all required clock lines. The clock rails used for these CMOS switches will be derived from the bias lines received from the Clock and Bias Board. The logic signals for the switches will come from the clock lines received from the Clock and Bias Board. Each clock line to individual CCDs will have a buffer driver.

Because we are using the generic Monsoon Transition Boards, all voltage protection devices will reside on the MIB.

Preamps will be included on MIB to drive the CCD video outputs to the CCD Acquisition Board.

The MIB will make use of daughter boards to allow us flexibility of design in clock driving, clock rail sharing, pre-amp usage, cable mapping, etc. The goal is to make it flexible enough to test a variety of possible configurations.



Block Diagram of Monsoon Test stand

For each CCD, we will supply the following:

INPUTS

HV: (supplied by external voltage reference)

Vsub

Bias Voltages: (supplied by CCD Acquisition Board – 32 bias settings available)

Vdd_u	Vdd_l
Vr_u	Vr_l
Vog_u	Vog_l

Clock Signals: (driven by CMOS switches on Monsoon Interface Board [MIB] and possible buffer outputs)

V1_u	V1_l
V2_u	V2_l
V3_u	V2_l
Tg_u	Tg_l
H1_u	H1_l
H2_u	H2_l
H3_u	H3_l
SW_u	SW_l
Rg_u	Rg_l

Guard Rails:

p+guard	(grounded)
n+guard	(usually floating – may need to be grounded for erase)

OUTPUTS

Video Outputs:

Vout_u	Vout_l

RTD Output:

RTDV+	RTDV-
RTDI+	RTDI-

Mapping of Monsoon Clock and Bias Board - LV Bias Signals for clock rails

LV Bias Signal (35:0)	Recommended Operating Value	Used for
0	+5V	V1_u, V1_l (high rail)
1	-3V	V1_u, V1_l (low rail)
2	+5V	V2_u, V2_l (high rail)
3	-3V	V2_u, V2_l (low rail)
4	+5V	V3_u, V3_l (high rail)
5	-3V	V3_u, V3_l (low rail)
6	+5V	Tg_u, Tg_l (high rail)
7	-3V	Tg_u, Tg_l (low rail)
8	+6V	H1_u, H2_u, H3_u (high rail)
9	-4V	H1_u, H2_u, H3_u (low rail)
10	+6V	H1_l, H2_l, H3_l (high rail)
11	-4V	H1_l, H2_l, H3_l (low rail)
12	+5V	SW_u (high rail)
13	-5V	SW_u (low rail)
14	+5V	SW_l (high rail)
15	-5V	SW_l (low rail)
16	0V	Rg_u (high rail)
17	-6V	Rg_u (low rail)
18	0V	Rg_l (high rail)
19	-6V	Rg_l (low rail)
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Mapping of Monsoon Clock and Bias Board - Clock Signals to CCD clocking rails

Clock Signal (31:0)	Used for logic level inputs to CMOS switches (0-5V or 0-3V)	Used to create below clock signal
0	logic level	V1_u, V1_l
1	logic level	V2_u, V1_2
2	logic level	V3_u, V1_3
3	logic level	Tg_u, Tg_l
4	logic level	H1_u
5	logic level	H1_l
6	logic level	H2_u
7	logic level	H2_l
8	logic level	H3_u
9	logic level	H3_l
10	logic level	SW_u
11	logic level	SW_l
12	logic level	RG_u
13	logic level	RG_l
14	logic level	Enabling Vdd_u and Vdd_l
15	logic level	Enabling Vr_u and Vr_l
16	logic level	Enabling Vog_u and Vog_l
17	logic level	Enables grounding of p+guard
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Mapping of Monsoon CCD Acquisition Board Bias levels to CCDs

Bias Output (31:0)	Recommended Operating Value	Used for
0	-22V	CCD_1 Vdd_u
1	-22V	CCD_1 Vdd_l
2	-12.5V	CCD_1 Vr_u
3	-12.5V	CCD_1 Vr_l
4	+2.2V	CCD_1 Vog_u
5	+2.2V	CCD_1 Vog_l
6	-22V	CCD_2 Vdd_u
7	-22V	CCD_2 Vdd_l
8	-12.5V	CCD_2 Vr_u
9	-12.5V	CCD_2 Vr_l
10	+2.2V	CCD_2 Vog_u
11	+2.2V	CCD_2 Vog_l
12	-22V	CCD_3 Vdd_u
13	-22V	CCD_3 Vdd_l
14	-12.5V	CCD_3 Vr_u
15	-12.5V	CCD_3 Vr_l
16	+2.2V	CCD_3 Vog_u
17	+2.2V	CCD_3 Vog_l
18	-22V	CCD_4 Vdd_u
19	-22V	CCD_4 Vdd_l
20	-12.5V	CCD_4 Vr_u
21	-12.5V	CCD_4 Vr_l
22	+2.2V	CCD_4 Vog_u
23	+2.2V	CCD_4 Vog_l
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Can bias outputs put out –22V?